## REMARKS

The Examiner's action dated December 17, 2003, has been received and its contents carefully noted. In view thereof, claim 5 has been amended in order to place the present application in condition for allowance. Support for this feature, for example, is shown in reference numerals 4s and 4d in Fig. 4 and discussed on page 14, lines 13-18 of the present application. As previously, claims 5 and 8-14 are presently pending in the instant application with claims 8-11 being withdrawn from further consideration by the Examiner. Applicants note with appreciation, the allowance of claims 12-14.

On page 2 of the Office Action, claim 5 is rejected under 35 U.S.C. 102(b) as being anticipated by Japanese Patent No. JP04062975A to Ishii. In view of the amendments provided above and the comments below, Applicants respectfully traverse this rejection.

The Ishii patent discloses a high voltage transistor including: a source diffusion region (corresponding to the source offset region of the present invention) composed of an n-type low-concentration impurity diffusion region 5, and a drain diffusion region (the drain offset region of the present invention) composed of another n-type low-concentration impurity diffusion region 5, and an n-type high-concentration impurity diffusion region 6.

On the other hand, the present invention as now set forth in independent claim 5, is directed to a high-voltage MOS transistor wherein a dopant concentration of a drain offset region is set independently of a dopant concentration of a source offset region in the entire drain offset region, and the dopant concentration of the source offset region is set lower than the dopant concentration of the drain offset region and thereby a resistance value of the source offset region is set independently of a resistance value of the drain offset region in such a manner as to maintain a high sustaining breakdown voltage of the high-voltage MOS transistor, which is based on a voltage of the source offset region and a voltage of a substrate region directly under a gate insulating film during operation of the high-voltage MOS transistor. Applicants submit that Ishii does not disclose or suggest this combination of features.

For example, in the transistor of the present invention, the dopant concentration of the drain offset region is set independently of that of the source offset region in the entire drain offset region. Thus, when the dopant concentration of the source offset region is set lower than that of the drain offset region and the resistance value of the source offset region increases, the dopant concentration of the entire drain offset region does not vary and the

resistance value thereof is not affected at all. Therefore, in the present invention, the dopant concentration and the resistance value of the drain offset region maintain a good current flow between the drain and the source, thereby avoiding the deterioration of the drive capacity of the transistor. Hence, the present invention achieves the effect of maintaining high sustaining breakdown voltage by independently setting the resistance value of the source offset region and that of the drain offset region.

Applicants submit that, contrary to the presently claimed invention, the drain diffusion region in the transistor of Ishii is composed of two diffusion regions having a different concentrations (the n-type low-concentration impurity diffusion region 5 and the n-type high-concentration impurity diffusion region 6). The dopant concentration of the source diffusion region is set lower than that of the drain diffusion region. Furthermore, Applicants submit that, in Ishii, the source diffusion region 5 appears to have the same dopant concentration as the n-type low-concentration impurity diffusion region 5 of the drain diffusion region since both regions are denoted by the same reference numeral (5) and both regions are formed in the same step.

Moreover, when the dopant concentration of the source diffusion region (5) of Ishii is set lower than that of the drain diffusion region to improve a sustaining breakdown voltage, the dopant concentration of the n-type low-concentration impurity diffusion region (5) also becomes low correspondingly. As a result, even if the n-type high-concentration impurity diffusion region (6) having a low resistance value is being formed, a resistance value of the entire drain diffusion region (5 and 6) may increase, causing a deterioration of a drive capacity of the transistor due to the reduction of the current flow between the drain and the source. Thus, within the transistor of Ishii, the resistance value of the drain diffusion region varies in association with a change of the resistance value of the source diffusion region, and the resistance value of the source diffusion region cannot be set independently of the resistance value of the drain diffusion region to maintain the high sustaining breakdown voltage.

Thus Applicants submit that, in the transistor disclosed in the Ishii patent, the dopant concentration of the drain diffusion region is <u>not</u> set independently of that of the source diffusion region in the entire drain diffusion region, but instead partially depends on that of the source diffusion region. Hence, Applicants respectfully submit that Ishii does not disclose or suggest that <u>the dopant concentration of the drain offset region is set independently of that</u>

of the source offset region in the entire drain offset region, as now set forth in independent claim 5 of the present invention.

Therefore, in view of the foregoing, it is respectfully requested that the rejections of record be reconsidered and withdrawn by the Examiner, that claim 5 be allowed and that the application be passed to issue.

Should the Examiner believe a conference would be of benefit in expediting the prosecution in the instant application, it is hereby invited to telephone counsel to arrange such a conference.

Respectfully submitted,

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